SIDDHARTH INSTITUTE OF ENGINEERING AND TECHNOLOGY :: PUTTUR
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QUESTION BANK (DESCRIPTIVE)

Subject with Code : VERILOG HDL(16EC5704)

Branch & specialization : MTECH-VLSI **Year & Sem:** I_M.Tech & I-Sem

UNIT –I

HARDWARE MODELING WITH THE VERILOG HDL

1. a) Explain structure design methodology with the verilog HDL. [5M]
   b) Write verilog HDC structural model for a full sub tractor using NAND gates. [5M]
2. a) Explain hardware modeling verilog primitives. [5M]
   b) Explain behavioral description in verilog. [5M]
3. Explain the following descriptive styles of system hardware with the verilog HDL
   a) Structural description. [5M]
   b) Behavioral description [5M]
4. a) Explain structured design methodology. [5M]
   b) Explain hierarchical descriptions of hardware. [5M]
5. a) Discuss various descriptive styles available for hardware modeling using verilog HDL. [5M]
   b) With neat flow graph, explain the TOP down design methodology relevant to hardware modeling using verilog HDL. [5M]
6. a) Explain the terms “Hardware Encapsulation” and “Hardware modeling” with suitable example using verilog HDL. [5M]
   b) Describe hierarchical description of hardware modeling using verilog HDL. [5M]
7. a) Explain about Arrays of Instances in verilog with an example. [5M]
   b) Write a brief notes on number representation in verilog. [5M]
8. a) Write a verilog program for 8x1 MUX using Structured Implicit model. [5M]
   b) Write a verilog program for Half adder using Structured Explicit model. [5M]
9. a) Explain any descriptive style of system hardware with the Verilog HDL with an example. [5M]
   b) Write a brief note on language conventions in verilog. [5M]
10. a) Write a brief note on Hardware Modeling Verilog Primitives. [5M]

b) Write a program using TOP down design methodology in verilog. [5M]

UNIT –II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL

1. Explain in detail about verilog HDC data types with suitable examples. [10M]
2. a) What is user defined primitives? Explain combinational behavior of user defined primitives. [7M]
   b) Explain conditional operator, operator precedence in VERILOG. [3M]
3. Explain following concepts.
   a) Verilog strings [3M]
   b) Verilog constants [2M]
   c) Verilog operations [3M]
   d) Verilog variables [3M]
4. a) Compare the combinational behavior and sequential behavior of user defined primitives. [5M]
   b) Explain the verilog model for net delay and module paths and delays. [5M]
5. a) Differentiate the combinational and sequential behavior of user-defined primitives for hardware modeling using verilog HDL. [5M]
   b) Present verilog models for transport delay with relevant examples. [5M]
6. a) Illustrate the initialization of sequential primitives with relevant examples. [5M]
   b) Explain the terms “Inertial delay” and “Transport delay” relevant to verilog HDL models with suitable examples. [5M]
7. Explain following concepts with example program.
   a) Verilog operators [5M]
   b) Verilog variables [5M]
8. Explain following concepts with example.
   a) Verilog Expressions and Operands [5M]
   b) Verilog Data Types [5M]
9. a) Write a brief short note on Path Delays and Simulation. [5M]
   b) Explain the following i) Inertial Delay Effects ii) Pulse Rejection [5M]
10. a) Write a brief short notes on User Defined Primitives in verilog. [5M]
    b) Explain Built-In Constructs for Delay in verilog. [5M]

UNIT –III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL

1. a) Explain behavioral statements in verilog HDC. [5M]
   b) Name two kinds of assignments that you can have in verilog HDC model and explain them. [5M]
2. a) Write short notes on non-blocking assignments and what are the sequences takes place at each positive edge of clock for the non-blocking assignments. [7M]
   b) Explain behavioral models of finite state machine. [3M]
3. a) Write a short note on intra assignment delay. [3M]
   b) Explain behavioral models of finite state machines. [7M]
4. a) How intra assignments delay control, event based timing control takes place in verilog HDL? [5M]
   b) Writ program for Moore machine in behavioral models. [5M]
5. a) Explain how to summarize the various delays constructs in hardware modeling with the verilog HDL. [5M]
   b) Explain the concept of 'constructs for activity flow control'. Give the behavioral description in verilog HDL. [5M]
6. a) Explain the behavioral descriptions for simulation of simultaneous procedural assignment used in verilog HDL with suitable example. [5M]
   b) Explain the Indeterminate Assignments and Ambiguity in verilog. [5M]
7. a) How the timing checks can be given in system tasks in verilog. [5M]
   b) Draw the ASM chart for the dice game and write a program in behavioral models verilog HDL [5M]
8. a) Write short notes on Simultaneous Procedural Assignments. [5M]
   b) What is the differences between an initial behavior and an always behavior [5M]
9. a) Give a Summary of Delay Constructs in Verilog. [5M]
   b) Write a short note on Variable Scope Revisited in verilog. [5M]
10. Explain the following.
    a) Procedural Continuous Assignments [5M]
    b) Procedural Assignment [5M]

UNIT –IV

SYNTHSIS OF COMBINATIONAL LOGIC

1. a) Draw the block diagram for HDL based synthesis explain each block [7M]
   b) Explain the tree state buffers. [3M]
2. a) Draw the block diagram for test bench for post synthesis design verifications. [7M]
   b) Discuss about behavioral synthesis. [3M]
3. a) Explain the block in the logical synthesis. [5M]
   b) Discuss about RTL synthesis. [5M]
4. a) Function of 'F" that is to be decomposed in terms of new nodes x & y the original form of f is described by the Boolean equation. [5M]

   $F=ABC+ABD+\overline{ACD}+\overline{BCD}$

   b) What is synthesis of priority structures give one examplewith program? [5M]
5. Explain the following. [5M]
   a) Simulation efficiency.
   b) Procedural continuous assignments [5M]
6. a) Write, verify and synth size a 16 bit adder sub tractor. [5M]
   b) Explain the synthesis of user defined function. [5M]
7. a) Write a program for synthesis of user defined tasks? [5M]
   b) Write a program for synthesis of case and conditional. [5M]
8. a) What is synthesis of the disable statements write any one program for it. [5M]
   b) Explain the non-blocking assignments of synthesis. [5M]
9. a) Draw the flow chart for synthesis of loops explain each block? [5M]
   b) Write program for synthesis of multi cycle operations. [5M]
10. a) write and explain the types of timing controls in synthesis. [7M]
    b) Explain the fork &join blocks. [3M]

UNIT –V

SWITCH-LEVEL MODELS IN VERILOG

1. a) Discuss why switch level is useful? [5M]

b) Give the MOS transistor technology? [5M]

2. a) Write and verify a switch level al a three input static CMOS NOR gate? [5M]

   b) Explain the true table for switch level MOSFET transistor module? [5M]

3. a) Write and verify the switch level al JK flip flop having preset and clear input? [5M]

   b) Draw the circuit diagram of CMOS and explain it? [5M]

4. a) Design & verify a switch level model at the four channel MOS transistor [7M]

   b) Discuss about alternative loads and pull gates? [3M]

5. a) Explain the CMOS transmission gates with diagram? [5M]

   b) Write a test bench and simulate the behavior at the circuit in fig. [5M]

6. a) Explain the types of signal strengths? [5M]

   b) Draw & explain the circuit diagram of CMOS switch with a program. [5M]

7. a) Discuss about Ambiguous signals? [5M]

   b) Write a program for NMOS Three input NOR gate? [5M]

8. Explain the following.

   a) Strength reduction by primitives [5M]

   b) Transistor switch & bi-directional switch [5M]

9. a) Design the circuit diagram for CMOS NOR gate? [3M]

   b) Implement NAND, AND, OR gates using MOS switch test it with a suitable test bench? [7M]

10. a) Write a program for NMOS inverter with pull up loads? [5M]

    b) Implement a 4X1 mux using CMOS transmission gates? [5M]

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